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09/943,068	08/29/2001	James Kent Heckman	W2K1062	8680

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EXAMINER
DOLAN, JENNIFER M

ART UNIT	PAPER NUMBER
2813	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/943,068	Applicant(s) HECKMAN ET AL.	
	Examiner Jennifer M. Dolan	Art Unit 2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

riod for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 November 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13 and 27-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13 and 27-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claim 2 is objected to because of the following informalities: In lines 1 and 2, "optical the integrated" should be replaced by --the optical integrated--. Appropriate correction is required.

2. Regarding claims 10-12 and 36-38, as the claims are directed to an optical integrated circuit, per se, the method limitations appearing in claims 10-12 and 36-38 have only been accorded weight to the extent that they affect the structure of the completed optical integrated circuit. Note that "determination of patentability in 'product-by-process' claims is based on product itself, even though such claims are limited and defined by process [i.e., "epitaxial growth", "etched metal" or "stamped metal"], and thus product in such claim is unpatentable if it is the same as, or obvious form, product of prior art, even if prior product was made by a different process", *In re Thorpe, et al.*, 227 USPQ 964 (CAFC 1985). Furthermore, note that a "product-by-process claim, although reciting subject matter of claim in terms of how it is made [i.e., "through epitaxial growth", "etching metal" or "stamping metal"] is still product claim; it is patentability of product claimed and not recited process steps that must be established, in spite of fact that claim may recite only process limitations", *In re Hirao and Sato*, 190 USPQ 685 (CCPA 1976). Note that in the instant case, an "epitaxially grown semiconductor layer" is not distinguishable from any crystalline semiconductor layer, and there is no distinguishability between a "stamped metal layer," an "etched metal layer," or simply a metal layer with

apertures. Hence, the product of claims 10 and 36 is simply a template that is a semiconductor layer, and the product of claims 11, 12, 37, and 38 is simply a template that is a metal layer, in addition to the limitations of claims 1 and 27.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

4. Claims 1, 3-6, 10, and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,824,186 to Smith et al.

Regarding claim 1, Smith discloses an optical integrated circuit (column 1, lines 22-56; column 13, lines 8-53), comprising: a substrate (50); a plurality of dies (205; 127); a template layer (53, 55) attached to a top side of the substrate (figures 6-10) for aligning the dies by contacting the dies during placement of the dies on the template layer and substrate (column 4, lines 17-42; figures 6-9).

Regarding claim 3, Smith discloses that the template layer has rectangular apertures for accepting the plurality of dies (figure 13).

Regarding claim 4, Smith discloses that the template layer has protrusions substantially perpendicular to the mounting surface of the substrate for guiding the dies during placement (figure 13).

Regarding claim 5, Smith discloses that the protrusions are tapered, having a narrow end farthest from the substrate, so that the dies may self-align as the dies are guided toward the substrate (figures 6-9, figure 15).

Regarding claim 6, Smith discloses that the template layer has rectangular apertures for accepting the plurality of dies, and wherein walls of the rectangular apertures are formed by the protrusions (figures 6-9 and 15).

Regarding claim 10, Smith discloses that the template layer is a semiconductor layer (figures 6-9).

Regarding claim 13, Smith discloses an optical integrated circuit (column 1, lines 22-56; column 13, lines 8-53), comprising: a substrate (50); a plurality of dies (205; 127); and means (template layer (53, 55) attached to a top side of the substrate (figures 6-10)) for aligning the dies during placement of the dies on the template layer and substrate (column 4, lines 17-42; figures 6-9).

5. Claims 1, 11, and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent Application No. 2002/0186477 to Wang et al.

Regarding claim 1, Wang discloses an optical integrated circuit (paragraph 0009), comprising: a substrate (150), a plurality of dies (200); and a template layer (100) attached to the

top side of the substrate for aligning the dies by contacting the dies during placement of the dies on the template layer and the substrate (figures 3 and 5).

Regarding claims 11 and 12, Wang discloses that the template layer is made of metal (paragraph 0002).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 2, 27-31, and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith et al. in view of U.S. Patent Application No. 2002/0180016 to Shrauger.

Regarding claim 2, Smith discloses optical integrated circuit dies (column 13, lines 8-52), but fails to disclose that the integrated circuit is a mirror array, and the dies are mirror sub-arrays.

Shrauger discloses an optical integrated circuit which is a mirror array, with dies that are mirror sub-arrays (paragraph 0008). Shrauger further teaches that with highly precise die alignment, many small mirror sub-arrays can be formed into a large mirror array (paragraphs 0008 and 0009).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the optical integrated circuit and template of Smith, so that it uses dies that are mirror sub-arrays, as taught by Shrauger. The rationale is as follows: A person having ordinary skill in the art would have been motivated to use mirror sub-arrays in place of the

optical IC dies of Smith, because the division of a mirror array into subarrays allows for a higher device yield and smaller device size, since only the known good parts need to be used in each subarray, providing that a very precise alignment between dies can be achieved (Shrauger, paragraphs 0008 and 0009). Since highly precise positioning of dies can be achieved with the template of Smith, it is well within the purview of a person having ordinary skill in the art to use mirror subarrays in the template of Smith.

Regarding claims 27 and 28, Smith discloses an optical integrated circuit (column 1, lines 22-56; column 13, lines 8-53), comprising: a substrate (50); a plurality of dies (205; 127); and means (template layer (53, 55) having rectangular apertures for receiving the plurality of dies, figure 13) attached to a top layer of the substrate (figures 6-10) for aligning the dies by contacting the dies during placement of the dies on the template layer and substrate (column 4, lines 17-42; figures 6-9).

Smith fails to disclose that the integrated circuit is a mirror array, and the dies are mirror sub-arrays.

Shrauger discloses an optical integrated circuit which is a mirror array, with dies that are mirror sub-arrays (paragraph 0008). Shrauger further teaches that with highly precise die alignment, many small mirror sub-arrays can be formed into a large mirror array (paragraphs 0008 and 0009).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the optical integrated circuit and template of Smith, so that it uses dies that are mirror sub-arrays, as taught by Shrauger. The rationale is as follows: A person having ordinary skill in the art would have been motivated to use mirror sub-arrays in the optical IC die

template of Smith, because the division of a mirror array into subarrays allows for a higher device yield and smaller device size, since only the known good parts need to be used in each subarray, providing that a very precise alignment between dies can be achieved (Shrauger, paragraphs 0008 and 0009). Since highly precise positioning of dies can be achieved with the template of Smith, it is well within the purview of a person having ordinary skill in the art to use mirror subarrays in the template of Smith.

Regarding claim 29, Smith discloses that the means has protrusions substantially perpendicular to the mounting surface of the substrate for guiding the dies during placement (figure 13).

Regarding claim 30, Smith discloses that the protrusions are tapered, having a narrow end farthest from the substrate, so that the dies may self-align as the dies are guided toward the substrate (figures 6-9, figure 15).

Regarding claim 31, Smith discloses that the template layer has rectangular apertures for accepting the plurality of dies, and wherein walls of the rectangular apertures are formed by the protrusions (figures 6-9 and 15).

Regarding claim 32, Smith discloses an adhesive layer (75) for attaching the plurality of dies to the substrate (column 13, lines 1-20).

Regarding claim 36, Smith discloses that the template layer is a semiconductor layer (figures 6-9).

8. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Smith et al. in view of U.S. Patent No. 5,298,791 to Liberty et al.

Smith discloses an adhesive layer (75) for attaching the dies to the substrate (column 13, lines 1-20), but fails to disclose that the adhesive layer is cut to provide vents to permit the escape of gas during mounting of the dies.

Liberty discloses an adhesive layer (1 or 42) which is cut to provide vents to permit the escape of gas during mounting of a circuit component to a heat sink or substrate (column 4, lines 54-58; column 6, lines 30-40).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the adhesive of Smith such that it is cut to provide vents, as taught by Liberty. The rationale is as follows: A person having ordinary skill in the art would have been motivated to provide vents in the adhesive, so that air bubbles can be removed from between the substrate and dies, such that heat generated in the die can be effectively dissipated in the substrate (Liberty, column 1, lines 17-40), the bond strength between the substrate and die is kept strong, rather than being weakened by air bubbles, and the substrate and die are not damaged by moisture retention.

9. Claim 33 rejected under 35 U.S.C. 103(a) as being unpatentable over Smith et al. in view of Shrauger, as applied to claim 32 above, and further in view of Liberty et al.

Smith fails to disclose that the adhesive is cut to provide vents to permit the escape of gas during mounting of the plurality of mirror arrays.

Liberty discloses an adhesive layer (1 or 42) which is cut to provide vents to permit the escape of gas during mounting of a circuit component to a heat sink or substrate (column 4, lines 54-58; column 6, lines 30-40).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the adhesive of Smith as modified by Shrauger, such that it is cut to provide vents, as taught by Liberty. The rationale is as follows: A person having ordinary skill in the art would have been motivated to provide vents in the adhesive, so that air bubbles can be removed from between the substrate and dies, such that heat generated in the die can be effectively dissipated in the substrate (Liberty, column 1, lines 17-40), the bond strength between the substrate and die is kept strong, rather than being weakened by air bubbles, and the substrate and die are not damaged by moisture retention.

10. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Smith et al. in view of U.S. Patent No. 6,490,166 to Ramalingam et al.

Smith fails to disclose perforations in the substrate.

Ramalingam discloses that the substrate has perforations for permitting the escape of gas during mounting of the dies (column 2, lines 33-41).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the substrate of Smith to include the perforations taught by Ramalingam. The rationale is as follows: A person having ordinary skill in the art would have been motivated to provide perforations in the substrate, because the perforations allow for the release of gas formed during the bonding process, which in turn strengthens the substrate/die interface, and protects the substrate from delamination or damages due to moisture absorption (Ramalingam, column 1, lines 30-44).

11. Claim 34 rejected under 35 U.S.C. 103(a) as being unpatentable over Smith et al. in view of Shrauger, as applied to claim 27 above, and further in view of Ramalingam et al.

Smith fails to disclose perforations in the substrate.

Ramalingam discloses that the substrate has perforations for permitting the escape of gas during mounting of the dies (column 2, lines 33-41).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the substrate of Smith as modified by Shrauger, to include the perforations taught by Ramalingam. The rationale is as follows: A person having ordinary skill in the art would have been motivated to provide perforations in the substrate, because the perforations allow for the release of gas formed during the bonding process, which in turn strengthens the substrate/die interface, and protects the substrate from delamination or damages due to moisture absorption (Ramalingam, column 1, lines 30-44).

12. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. in view of U.S. Patent No. 5,368,880 to McKee et al.

Wang discloses that the template layer is bonded to the substrate (paragraphs 0035, 0036), but fails to disclose that the bonding is through a eutectoid layer.

McKee discloses bonding two structures using a eutectoid layer (column 1, lines 5-22).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the optical integrated circuit of Wang such that the template is bonded to the substrate through a eutectoid layer, as suggested by McKee. The rationale is as follows: A person having ordinary skill in the art would have been motivated to bond the template and

substrate with a eutectoid layer, because a eutectoid layer provides precise parallelism between the substrate and template (McKee, column 1, lines 5-22), which would increase the accuracy of die placement in the template, as well as providing a strong and temperature-resistant bond that would not break upon die mounting, as is appreciated by one skilled in the art.

13. Claims 27, 37, and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. in view of Shrauger et al.

Regarding claim 27, Wang discloses an optical integrated circuit (paragraph 0009), comprising: a substrate (150), a plurality of dies (200); and means (template layer (100)) attached to a top layer of the substrate for aligning the dies by contacting the dies during placement of the dies on the template layer and the substrate (figures 3 and 5). Wang discloses that the dies may comprise mirrors or MEMS, but does not specify mirror sub-arrays.

Shrauger discloses an optical integrated circuit which is a mirror array, with dies that are mirror sub-arrays (paragraph 0008). Shrauger further teaches that with highly precise die alignment, many small mirror sub-arrays can be formed into a large mirror array (paragraphs 0008 and 0009).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the optical integrated circuit and template of Wang, so that it uses dies that are mirror sub-arrays, as taught by Shrauger. The rationale is as follows: A person having ordinary skill in the art would have been motivated to use mirror sub-array dies in the die template of Wang, because the division of a mirror array into subarrays allows for a higher device yield and smaller device size, since only the known good parts need to be used in each

subarray, providing that a very precise alignment between dies can be achieved (Shrauger, paragraphs 0008 and 0009). Since precise positioning of dies can be achieved with the template of Wang, and since Wang already suggests the use of MEMS or mirror dies, it is well within the purview of a person having ordinary skill in the art to use mirror subarrays in the template of Wang.

Regarding claims 37 and 38, Wang discloses that the template layer is made of metal (paragraph 0002).

14. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. in view of Shrauger, as applied to claim 27, above, and further in view of McKee.

Wang discloses that the template layer is bonded to the substrate (paragraphs 0035, 0036), but fails to disclose that the bonding is through a eutectoid layer.

McKee discloses bonding two structures using a eutectoid layer (column 1, lines 5-22).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the optical integrated circuit of Wang as modified by Shrauger, such that the template is bonded to the substrate through a eutectoid layer, as suggested by McKee. The rationale is as follows: A person having ordinary skill in the art would have been motivated to bond the template and substrate with a eutectoid layer, because a eutectoid layer provides precise parallelism between the substrate and template (McKee, column 1, lines 5-22), which would increase the accuracy of die placement in the template, as well as providing a strong and temperature-resistant bond that would not break upon die mounting, as is appreciated by one skilled in the art.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent Publication No. 2002/0110312 to Yang et al. discloses a method for mounting a mirror array on a substrate.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (703) 305-3233. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (703) 305-4940. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Jennifer M. Dolan
Examiner
Art Unit 2813

jmd
January 24, 2003

Carl Whitehead

CARL WHITEHEAD, JR.
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